26.1 A 750mV 15kHz 1/f Noise Corner 51dBm IIP2 Direct-Conversion Front-End for GSM in 90nm CMOS

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The dynamic range, required by wireless cell-phone terminals, makes the design of analog circuits at the supply voltage available in deep submicron CMOS technologies so challenging that researchers are investigating alternative methods to process the received signal [1]. On the other hand, several analog techniques, at RF in particular, have emerged in the recent past, improving both linearity and noise performances of different building blocks, due to an in-depth understanding of the underlying physical processes [2, 3]. In this paper, a direct-conversion fully integrated RF front-end is proposed for GSM. Realized in 90nm CMOS, the chip operates at a supply voltage compatible with the 45nm node and demonstrates the following main performances: 3.5dB NF integrated between 1kHz and 100kHz, 15kHz 1/f noise corner, 51dBm minimum IIP2, at a supply voltage as low as 750mV. No calibration is required to meet the IIP2 specification.

GSM is particularly demanding due to closely spaced channels and huge interferers surrounding the received signal. The resulting required 1/f noise corner and IIP2 usually suggests disregarding a direct-conversion architecture when the technology is CMOS, despite its attractiveness to arrive at a highly integrated transceiver implementation. The RF front-end can not rely on any frequency selectivity, having the most dangerous interferers only few MHz away from the received signal. As pointed out in Fig. 26.1.1, the down-converter is the most critical block where low 1/f noise and high linearity are conflicting requirements, at given current consumption [3, 4]. Furthermore, the reduction in the available supply voltage of scaled processes calls for minimum device stacking, making a conventional Gilbert cell not attractive. In particular, a fully differential transconductor, though showing excellent IIP2 performances, determines a significant voltage drop to accommodate the biasing current source. The pseudo-differential alternative has the advantage of a lower voltage drop and a superior IIP3, though at the expense of a dramatically reduced IIP2. The second-order common-mode conductance gain is at the origin of much higher second-order inter-modulation products in the mixer output current [4]. The idea proposed in this paper is to minimize the inter-modulation current produced by a pseudo-differential transconductor by means of a feedback loop controlling the mixer output common-mode voltage. Referring to Fig. 26.1.2, where the mixer schematic is drawn, an opamp senses the difference between the common-mode output voltage and a reference and drives the PMOS device, P_{CM}, supplying the common-mode current to the input transconductor. By inspection, the loop gain (G_{loop}) is given by:

$$G_{loop} = \frac{1}{2} A \cdot g_{m,P_{CM}} \cdot \left(R_1 \| r_{ds,P_L} \right) \quad (1)$$

where A is the opamp gain, $g_{m,PCM}$ is the tranconductance of P_{CM}, and $r_{ds,PL}$ the output resistance of P_L.

The loop operates at a low frequency and can produce a large gain at minimum consumption, significantly reducing the common-mode inter-modulation current injected into the switching pair. To gain quantitative insight, the effect of the transconductor inter-modulation current has to be considered in more detail. The common-mode current can be converted into a differential voltage at mixer output due to mismatches in the output resistors, or into a differential output current due to different dc leakage gains in the two switching pairs. Considering the typical IIP2 of a pseudo-differential transconductor is in the range of 0dBm to 5dBm, and both mismatches between resistors and switching pair leakage gains can be kept around -50dB at best, the resulting mixer IIP2, without the feedback control, is lower than 55dBm. This is absolutely inadequate for cell-phone applications. On the contrary, a further reduction of 40dB in the inter-modulating current, easily contributed by the feedback loop, increases IIP2 to better than 90dBm.

The load current source is realized by shunting the active device P_L with resistor R_1, in order to save voltage room while assuring matching between the common-mode load resistances.

The switching pair, set with the L_1-C_1 filter, is highly linear [2]. Despite the effectiveness of the filter reducing the 1/f noise contribution, the GSM baseband signal spectrum occupies only 100kHz, requiring a comparatively low noise corner which is extremely challenging in a sub-micron CMOS implementation. Given the margin in linearity, the strategy is trading IIP2 and IIP3 for 1/f noise by increasing the front-stage gain. The LNA, shown in Fig. 26.1.3, is a conventional inductively degenerated topology. Results are refined by means of simulations to meet targets. The LNA peak gain is 23dB while the mixer input-stage transconductance is 24mS. The implementation is tailored to PCS 1900.

The front-end, fabricated in a 90nm CMOS process, is housed in a plastic package. Figure 26.1.4 shows the chip micrograph. The core cell occupies 2.7mm^2. To minimize mismatches, active and passive mixer devices are interdigitated. LNA and mixer RF transistors are isolated in p-wells connected to a dedicated ground to avoid noise coupling from the substrate.

The circuit draws 15mA, 5mA by the LNA and 5mA by each mixer, from a 750mV supply. Figure 26.1.5 shows the simulated and measured RF gain and S_{11} magnitude. Gain is detected in-band, at 10kHz, and the -3dB output bandwidth is 650kHz. LO power is 4dBm. Figure 26.1.6 shows the input-referred noise power spectral density, demonstrating a 1/f noise corner as low as 15kHz. When averaged between 1kHz and 100kHz, the NF is 3.5dB. Second-order inter-modulation is tested injecting two tones 10kHz apart, at 6MHz from the received signal to emulate the AM blocker specified by the standard. IIP2 depends on mismatches among nominally identical devices. Because variations are expected, 25 samples are characterized. A maximum value of 68dBm is found while the minimum of 51dBm is still above requirement. Measured IIP3 is -10.5dBm. Figure 26.1.7 summarizes the results.

Even though designed to work at a supply of 750mV, it is still functional at 550mV: the peak gain reduces to 26dB, average NF is still 3.5dB while 3 samples show IIP2 below requirement.

Acknowledgment:
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References:
[1] A. A. Abidi, "RF CMOS Comes of Age," *IEEE J. Solid-State Circuits*, vol. 39, pp. 549-561, Apr., 2004
[2] M. Brandolini et al. "A CMOS Direct Down-converter with +78dBm Minimum IIP2 for 3G Cell-Phones," *ISSCC Dig. Tech. Papers*, vol. 48, pp. 320-321, Feb., 2005
[3] H. Darabi, A. Abidi, "Noise in RF-CMOS Mixers: A Simple Physical Model," *IEEE J. Solid-State Circuits*, vol. 35, pp. 15-25, Jan., 2000
[4] D. Manstretta et al. "Second-Order Intermodulation Mechanisms in CMOS Downconverters," *IEEE J. Solid-State Circuits*, vol. 38, pp. 394-406, Mar., 2003.

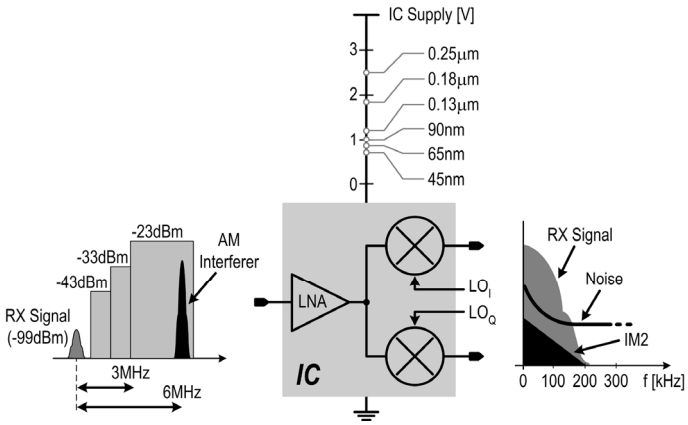

Figure 26.1.1: Challenges in a direct-conversion receiver front-end for GSM in sub-scaled CMOS.

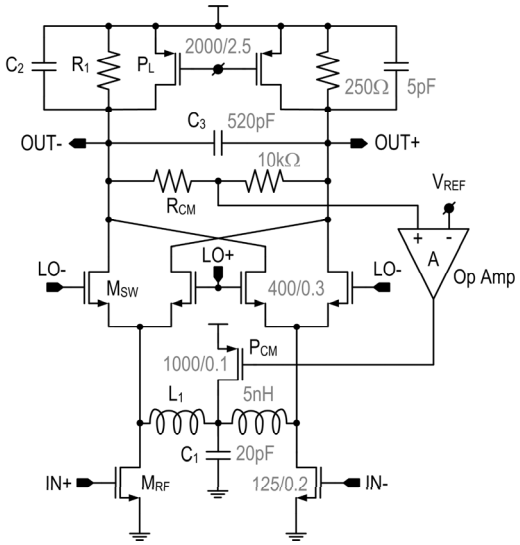

Figure 26.1.2: Mixer schematic.

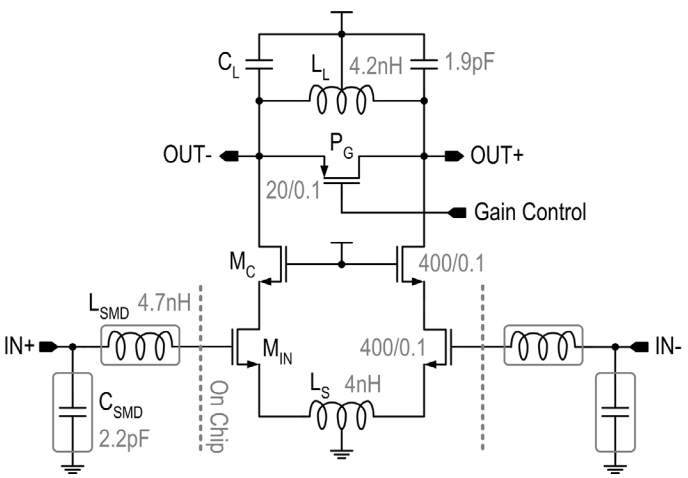

Figure 26.1.3: LNA schematic.

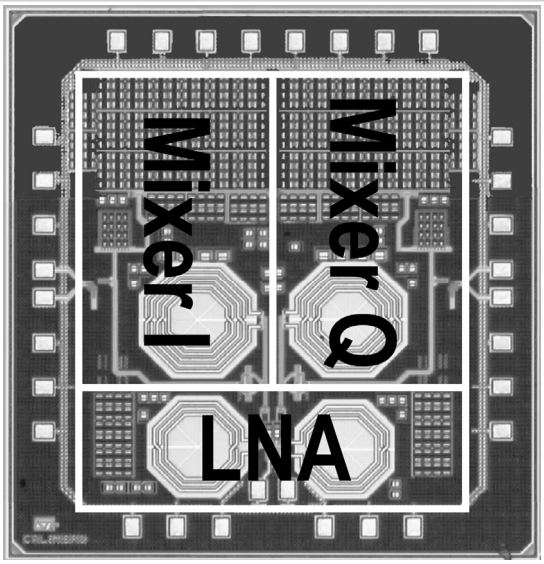

Figure 26.1.4: Die micrograph.

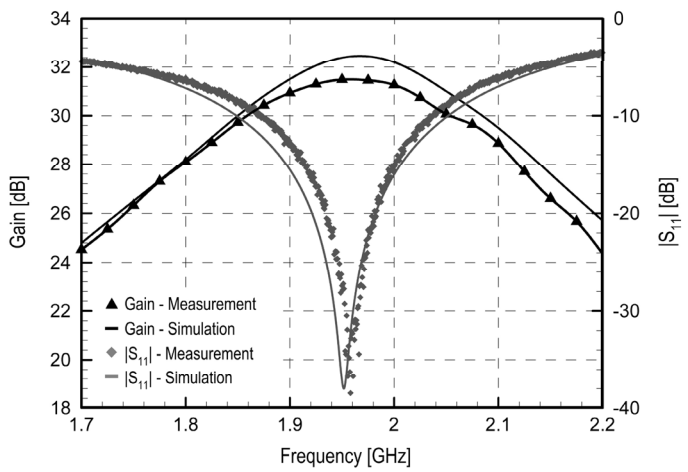

Figure 26.1.5: Measured and simulated front-end gain and $|S_{11}|$ versus input frequency.

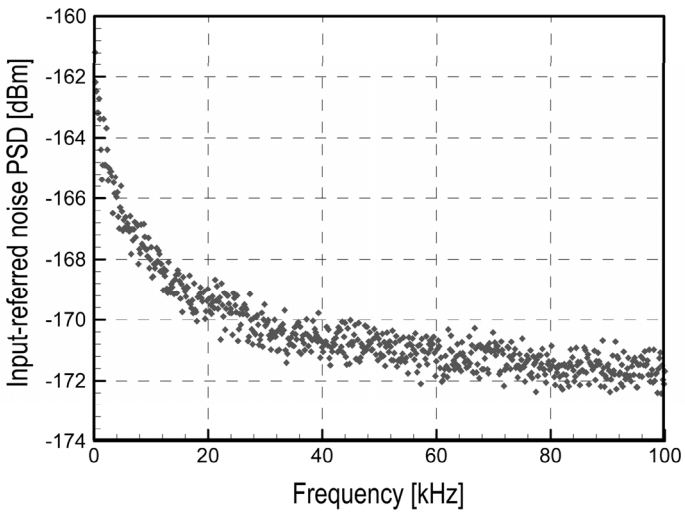

Figure 26.1.6: Measured input-referred noise power spectral density.

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Voltage Gain [dB]	31.5
Noise Figure [dB]	3.5
1/f Noise Corner [kHz]	15
Minimum IIP2 [dBm]	51
IIP3 [dBm]	-10.5
Gain Reduction [dB]	6
Voltage Supply [V]	0.75
Current consumption [mA]	15
Die area [mm^2]	4.3
Active area [mm^2]	2.7
Package	LQFP 32
Technology	90nm CMOS

Figure 26.1.7: Measurement summary.

